AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A predriver circuit comprising:

a pull-up circuit having at least one pull-up device of a first device type; and

a pull-down circuit ~~having~~ including at least one pull-down device of the first device type having a source coupled to ground, the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair.

2. (Original) The predriver circuit of claim 1, wherein the pull-up device is cross-coupled to the pull-down device.

3. (Original) The predriver circuit of claim 1, wherein the pull-up device and the pull-down device comprise NMOS devices.

4. (Original) The predriver circuit of claim 1, wherein the pull-up circuit comprises:

a first pull-up device having a gate coupled to a data input signal, a drain coupled to a power supply and a source coupled to the output node; and

a second pull-up device having a gate coupled to a complement input signal, a drain coupled to the power supply and a source coupled to the complement output node.

5. (Original) The predriver circuit of claim 1, wherein the pull-down circuit comprises:

a first pull-down device having a gate coupled to a complement input signal, a drain coupled to the output node and a source coupled to ground; and

a second pull-down device having a gate coupled to a data input signal, a drain coupled to the complement output node and a source coupled to ground.

6. (Original) The predriver circuit of claim 1, wherein the pull-down circuit further comprises:

a first device coupled between the output node and ground; and

a second device coupled between the complement output node and ground.

7. (Original) The predriver circuit of claim 6, wherein the first device comprises:

a gate and a drain coupled to the output node; and

a source coupled to ground.

8. (Original) The predriver circuit of claim 6, wherein the second device comprises:

a gate and a drain coupled to the complement output node and a source coupled to ground.

9. (Original) The predriver circuit of claim 2, further comprising:

a first pull-up device cross-coupled to a first pull-down device to receive a data input signal and to charge the output node and the complement output node in opposite directions; and

a second pull-up device cross-coupled to a second pull-down device to receive a complement data input signal and to charge the output node and the complement output node in opposite directions to generate the differential predriver signal pair.

10. (Original) The predriver circuit of claim 1, wherein the first and second pull-up devices comprise NMOS devices and the first and second pull-down devices comprise NMOS devices.

11. (Currently Amended) An output driver circuit, comprising:

a pull-up circuit having at least one pull-up device of a first device type; and

a pull-down circuit ~~having~~ including at least one pull-down device of the first device type having a source coupled to ground, the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair.

12. (Original) The output driver circuit of claim 11, wherein the pull-up device is cross-coupled to the pull-down device.

13. (Original) The output driver circuit of claim 11, wherein the pull-up device and the pull-down device comprise NMOS devices.

14. (Original) The output driver circuit of claim 11, wherein the pull-up circuit comprises:

a first pull-up device having a gate coupled to a data input signal, a drain coupled to a power supply and a source coupled to the output node; and

a second pull-up device having a gate coupled to a complement input signal, a drain coupled to a power supply and a source coupled to the complement output node.

15. (Original) The output driver circuit of claim 11, wherein the pull-down circuit comprises:

a first pull-down device having a gate coupled to a complement input signal, a drain coupled to the output node and a source coupled to ground; and

a second pull-down device having a gate coupled to a data input signal, a drain coupled to the complement output node and a source coupled to ground.

16. (Original) The output driver circuit of claim 11, wherein the pull-down circuit further comprises:

a first device coupled between the output node and ground; and

a second device coupled between the complement output node and ground.

17. (Original) The output driver circuit of claim 16, wherein the first device comprises:

a gate and a drain coupled to the output node; and

a source coupled to ground.

18. (Original) The output driver circuit of claim 16, wherein the second device comprises:

a gate and a drain coupled to the complement output node and a source coupled to ground.

19. (Original) The output driver circuit of claim 12, further comprising:

a first pull-up device cross-coupled to a first pull-down device to receive a data input signal and to charge an output node and a complement output node in opposite directions; and

a second pull-up device cross-coupled to a second pull-down device to receive a complement data input signal and to charge the output node and the complement output node in opposite directions to generate the differential predriver signal pair.

20. (Original) The output driver of claim 11, wherein the first and second pull-up devices comprise NMOS devices and the first and second pull-down devices comprise NMOS devices.

21. (Currently Amended) An electronic system comprising:

a printed wiring board on which a serial bus is formed, an integrated circuit (IC) chip package being operatively installed on the board to communicate using the serial bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the serial bus, the I/O section having an output driver in which a pre-driver includes a pull-up circuit having at least one pull-up device of a first device type, and a pull-down circuit having at least one pull-down device of the first device type, the pull-up circuit and the

pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair to open/close a pair of line driver switches to generate a differential output driver signal pair,

wherein the pull-up device is cross-coupled to the pull-down device.

22. (Original) The electronic system of claim 21, wherein the logic function section is a microprocessor.

23. (Original) The electronic system of claim 21, wherein the logic function section is a memory controller.

24. (Original) The electronic system of claim 21, wherein the logic function section is a bus bridge.

25. (Original) The electronic system of claim 21, wherein the logic function section is an I/O controller.

26. (Currently Amended) An article comprising a machine readable carrier medium carrying data which, when loaded into a computer system memory in conjunction with simulation routines, provides functionality of a model comprising:

a pull-up circuit having at least one pull-up device of a first device type; and

a pull-down circuit ~~having~~ including at least one pull-down device of the first device type having a source coupled to ground, the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair.

27. (Original) The article of claim 26, wherein the pull-down device is cross-coupled to the pull-down device.

28. (Original) The article of claim 26, wherein the pull-up device and the pull-down device comprise NMOS devices.

29. (Original) The article of claim 26, further comprising:

a first pull-up device cross-coupled to a first pull-down device to receive a data input signal; and

a second pull-up device cross-coupled to a second pull-down device to receive a complement data input signal.

30. (Original) The article of claim 26, wherein the first and second pull-up devices comprise NMOS devices and the first and second pull-down devices comprise NMOS devices.